AMENDMENTS TO THE CLAIMS

1. (Currently amended) A content addressable memory (CAM) comprising:

a CAM array that stores entries in P memory locations that each have a location width; the CAM array providing, for each location, a match signal indicating whether the location has a stored entry satisfying a match criterion;

match combining circuitry that responds to the match signals and to a signal indicating a search width that is a multiple of the location width, the match combining circuitry providing P/Q combined match signals, each combined match signal indicating a combination of a group of Q match signals, the combination depending on the indicated search width;

priority encoder circuitry that responds to the combined match signals, providing P/Q priority signals indicating at most one combined match signal that has priority and is asserted; and

search results circuitry that responds to the priority signals, providing search results signals indicating results of the search at the indicated search width.

2. (Original) The CAM of claim 1 in which the search results include an address code.

3. (Original) The CAM of claim 1 in which the search results include an array match signal.

4. (Original) The CAM of claim 1 in which the location width is 80 bits and the search width is one of 80, 160, and 320 bits.

5. (Currently amended) A content addressable memory (CAM) comprising:

a CAM array that stores entries in P memory locations that each have a location width; the CAM array providing match signals indicating whether locations have stored entries satisfying a match criterion; and

priority encoder circuitry that responds to the CAM array, providing P/Q priority signals indicating at most one Q group of two or more memory locations, the group storing an entry that has a search width greater than the location width, the entry having priority and meeting the match criterion.

6. (Original) The CAM of claim 5 in which each group of memory locations includes four memory locations, the search width being twice or four times the location width.

7. (Currently amended) A content addressable memory (CAM) comprising:

a CAM array that stores entries in P memory locations that each have a location width; the CAM array providing, for each location, a match signal indicating whether the location has a stored entry satisfying a match criterion;

match combining circuitry that responds to the match signals and to a signal indicating one of a set of search widths that are multiples of the location width;

the match combining circuitry providing P/Q combined match signals, each indicating a combination of Q match signals for a group of memory locations, the combination depending on the indicated search width; and

priority encoder circuitry that responds to the combined match signals, providing priority signals indicating at most one combined match signal's group of

memory locations; the indicated group storing an entry of the indicated search width that has priority and meets the match criterion.

8. (Original) The CAM of claim 7 in which each combined match signal is for a respective group of four memory locations, the search width being once, twice, or four times the location width.

9. (Currently amended) A content addressable memory (CAM) comprising:

a CAM array that stores entries in P memory locations that each have a location width; the CAM array providing match signals indicating whether locations have stored entries satisfying a match criterion;

priority encoder circuitry that responds to the CAM array, providing P/Q priority signals indicating at most one Q group of two or more memory locations, the indicated Q group storing an entry that has a search width that is a multiple of the location width, the entry having priority and meeting the match criterion; and

selection circuitry that responds to the priority signals, providing selected information for entries stored in the indicated group of two or more memory locations.

10. (Original) The CAM of claim 9 in which the selection circuitry provides selected information that includes match signals.

11. (Original) The CAM of claim 9 in which the CAM array also stores a suppress value for each memory location, the CAM array further providing suppress signals based on the locations' suppress values, the selection circuitry providing selected information that includes suppress signals.

12. (Original) The CAM of claim 9 in which each group of memory locations includes four memory locations, the search width being once, twice, or four times the location width.

13. (Currently amended) A content addressable memory (CAM) comprising:

a CAM array that stores entries in P memory locations that each have a location width and that stores, for each memory location, a suppress value; the CAM array providing match signals indicating whether locations have stored entries satisfying a match criterion and suppress signals based on locations' suppress values;

priority encoder circuitry that responds to the CAM array, providing P/Q priority signals indicating at most one Q group of two or more memory locations, the indicated Q group storing an entry that has a search width that is a multiple of the location width, the entry having priority and meeting the match criterion;

selection circuitry that responds to the priority signals, providing selected match signals and selected suppress signals for the indicated group of two or more memory locations; and

search results circuitry that responds to the selected match signals and the selected suppress signals, providing output search results.

14. (Original) The CAM of claim 13 in which the search results include an address code.

15. (Original) The CAM of claim 13 in which the search results include an array match signal.

16. (Original) The CAM of claim 13 in which each group of memory locations includes four memory locations, the search width being once, twice, or four times the location width.

17. (Currently amended) A content addressable memory (CAM) comprising:

a CAM array that stores entries in P memory locations; the CAM array providing, for each location, a match signal indicating whether the location has a stored entry satisfying a match criterion;

match combining circuitry that responds to the match signals and to a signal indicating one of a set of search widths; the match combining circuitry providing P/Q combined match signals, each indicating a combination of Q match signals for a group of two or more memory locations, the combination depending on the indicated search width; and

search results circuitry that responds to the combined match signals and to the signal indicating one of the set of search widths, providing an address code of a memory location in one of the groups of two or more locations, the memory location storing at least part of an entry of the indicated search width that satisfies the match criterion.

18. (Original) The CAM of claim 17 in which the search results circuitry includes a priority encoder that prioritizes the combined match signals.

19. (Original) The CAM of claim 17 in which each group of memory locations includes four memory locations.

20. (Original) A content addressable memory (CAM) comprising:

a CAM array that stores entries in memory locations that each have a location width and that stores, for each memory location, a suppress value; the CAM array providing, for each location, a match signal indicating whether the location has a stored entry satisfying a match criterion and a suppress signal based on the location's suppress value;

address code circuitry that responds to the match signals and to a signal indicating a search width that is one of a set of two or more multiples of the location width, providing an address code indicating one of a group of two or more memory locations, the group storing entries of each of the location widths in the set; the location indicated by the address code storing at least part of an entry of the indicated search width that satisfies the match criterion; and

array match circuitry that responds to the address code and to suppress signals for the group of memory locations; the array match circuitry providing an array match signal that is asserted only when no suppress signal is asserted for the entry.

21. (Original) The CAM of claim 20 in which the search width is once, twice, or four times the location width.

22. (Original) A content addressable memory (CAM) comprising:

a CAM array that stores entries in P memory locations that each have a location width and that stores, for each memory location, a suppress value; the CAM array providing, for each location, a match signal indicating whether the location has a stored entry satisfying a match criterion and a suppress signal based on the location's suppress value;

match combining circuitry that responds to the match signals and to a signal indicating a search width that is a multiple of the location width; the match combining circuitry providing P/Q combined match signals, each combined match signal indicating a combination of a respective group of Q match signals, the combination depending on the indicated search width;

priority encoder circuitry that responds to the combined match signals, providing P/Q priority signals, each priority signal indicating, for a respective combined match signal, whether it has priority and is asserted; the priority encoder circuitry also providing a PE match signal indicating whether any of the combined match signals is asserted;

match selecting circuitry that responds to the priority signals, selecting the respective group of Q match signals of the combined match signal that has priority and is asserted;

MSB address encoding circuitry that responds to the priority signals, providing $\log_2(P/Q)$ most significant bits (MSBs) of a $(\log_2 P)$-bit address code for the respective memory locations of the selected group of match signals;

LSB circuitry that responds to the selected group of match signals and to the signal indicating the search width; the LSB circuitry providing $\log_2 Q$ least significant bits (LSBs) of the address code, the address code being for a memory location of one of the selected group of match signals, the memory location storing at least part of an entry of the indicated search width that satisfies the match criterion; and

suppress selecting circuitry that responds to the priority signals, selecting a group of Q suppress signals for the respective memory locations of the selected group of match signals; and

array match circuitry that responds to the LSBs of the address code, the selected group of suppress signals, and the PE match signal; the array match circuitry providing an array match signal that is asserted only when the PE match signal is asserted and no suppress signal is asserted for the entry.

23. (Original) The CAM of claim 22 in which P is 1024 and Q is 4.

24. (Original) The CAM of claim 22 in which the location width is 80 bits and the search width is one of 80, 160, and 320 bits.

25. (Original) The CAM of claim 22 in which Q is 4 and in which the match combining circuitry includes:

first combiner circuitry that combines first and second match signals in accordance with the indicated search width to obtain a first intermediate signal;

second combiner circuitry that combines third and fourth match signals in accordance with the indicated search width to obtain a second intermediate signal; and

third combiner circuitry that combines the first and second intermediate signals in accordance with the indicated search width to obtain a combined match signal.

26. (Original) The CAM of claim 22 in which the match selecting circuitry includes Q dynamic logic circuits, each for selecting one match signal.

27. (Original) The CAM of claim 22 in which the suppress selecting circuitry includes Q dynamic logic circuits, each for selecting one suppress signal.

28. (Currently amended) A method of searching a content addressable memory (CAM) in which each memory location has a location width for its stored entry; the method comprising:

obtaining match signals, each match signal indicating whether a respective location in the CAM has a stored entry satisfying a match criterion; and

obtaining P/Q priority signals indicating at most one Q group of two or more memory locations, the group storing an entry that has a search width greater than the location width, the entry having priority and meeting the match criterion.

29. (Currently amended) A method of searching a content addressable memory (CAM) in which each memory location has a location width for its stored entry; the method comprising:

obtaining P match signals, each match signal indicating whether a respective location has a stored entry satisfying a match criterion;

in response to the match signals and to a signal indicating one of a set of search widths that are multiples of the location width, providing P/Q combined match signals; each combined match signal indicating a combination of Q match signals for a group of memory locations, the combination depending on the indicated search width; and

in response to the combined match signals, providing P/Q priority signals indicating at most one combined match signal's group of memory locations, the

indicated group storing an entry of the indicated search width that has priority and meets the match criterion.

30. (Currently amended) A method of searching a content addressable memory (CAM) in which each memory location has a location width for its stored entry; the method comprising:

obtaining match signals, each match signal indicating whether a respective location has a stored entry satisfying a match criterion;

obtaining P/Q priority signals indicating at most one Q group of two or more memory locations, the indicated group storing an entry that has a search width that is a multiple of the location width, the entry having priority and meeting the match criterion; and

in response to the priority signals, providing selected information for entries stored in the indicated group of two or more memory locations.

31. (Currently amended) A method of operating a content addressable memory (CAM); the method comprising:

obtaining, for each P location, a match signal indicating whether the location has a stored entry satisfying a match criterion; and

in response to the match signals and to a signal indicating one of a set of search widths, providing P/Q combined match signals, each combined match signal indicating a combination of Q match signals for a group of two or more memory locations, the combination depending on the indicated search width; and

in response to the combined match signals and to the signal indicating one of the set of search widths, providing an address code of a memory location in one of the groups of two or more locations, the memory location storing at least part of an entry of the indicated search width that satisfies the match criterion.

32. (Original) A method of operating a content addressable memory (CAM) in which each memory location has a location width for its stored entry and each memory location stores a suppress value for its stored entry; the method comprising:

obtaining match signals and suppress signals for memory locations, each match signal indicating whether a respective location has a stored entry satisfying a match criterion, each suppress signal being based on a respective location's stored suppress value;

in response to the match signals and to a signal indicating a search width that is one of a set of two or more multiples of the location width, providing an address code indicating one of a group of two or more memory locations, the group storing entries of each of the location widths in the set; the location indicated by the address code storing at least part of an entry of the indicated search width that satisfies the match criterion; and

in response to the address code and to suppress signals for the group of memory locations, providing an array match signal that is asserted only when no suppress signal is asserted for the entry.

33. (Currently amended) A method of operating a content addressable memory (CAM) in which each memory location has a location width for its stored entry

and each memory location stores a suppress value for its stored entry; the method comprising:

receiving search data indicating a match criterion;

obtaining P match signals and suppress signals for memory locations in the CAM, each match signal indicating whether a respective memory location has a stored entry satisfying the match criterion, each suppress signal being based on a respective memory location's stored suppress value;

in response to the match signals and to a signal indicating a search width that is a multiple of the location width, providing P/Q combined match signals, each combined match signal indicating a combination of a respective Q group of match signals, the combination depending on the indicated search width; in response to the combined match signals, providing priority signals indicating, for each combined match signal, whether it has priority and is asserted and also providing a PE match signal indicating whether any of the combined match signals is asserted;

in response to the priority signals, selecting the respective group of match signals and a group of suppress signals for respective locations of the group of match signals whose combined match signal has priority and is asserted, and also providing most significant bits (MSBs) of an address code for the respective memory locations of the selected group of match signals;

in response to the selected group of match signals and to the signal indicating the search width, providing least significant bits (LSBs) of the address code, the address code being for a memory location of one of the selected group of match signals, the

memory location storing at least part of an entry of the indicated search width that satisfies the match criterion; and

in response to the LSBs of the address code, the selected group of suppress signals, and the PE match signal, providing an array match signal that is asserted only when no suppress signal is asserted for the entry.

34. (Currently amended) An integrated circuit comprising:

a substrate with a surface;

content addressable memory (CAM) circuitry formed at the substrate's surface, including:

a CAM array that stores entries in P memory locations that each have a location width; the CAM array providing, for each location, a match signal indicating whether the location has a stored entry satisfying a match criterion;

match combining circuitry that responds to the match signals and to a signal indicating a search width that is a multiple of the location width, providing P/Q combined match signals, each combined match signal indicating a combination of a respective group of Q match signals, the combination depending on the indicated search width;

priority encoder circuitry that responds to the combined match signals, providing priority signals indicating at most one combined match signal that has priority and is asserted; and

search results circuitry that responds to the priority signals, providing search results signals indicating results of the search at the indicated search width.

35. (Currently amended) An integrated circuit comprising:

a substrate with a surface;

content addressable memory (CAM) circuitry formed at the substrate's surface, including:

a CAM array that stores entries in P locations that each have a location width and, for each entry, a suppress value; the CAM array receiving a search data item indicating a match criterion, and providing, for each location, a match signal indicating whether a data item that satisfies the match criterion is stored in the location and a suppress signal based on the location's suppress value; the CAM array including a lower part and an upper part, the lower part and the upper part being separated from each other on the substrate's surface;

match combining circuitry that responds to the match signals and to a signal indicating one of a set of search widths that are multiples of the location width, providing P/Q combined match signals, each combined match signal indicating a combination of a respective group of Q match signals, the combination depending on the indicated search width;

priority encoder circuitry that responds to the combined match signals, providing P/Q priority signals indicating at most one combined match signal that is asserted and has priority and also providing a PE match signal indicating whether any of the combined match signals is asserted; and

search results circuitry that responds to the match signals, the priority signals, and the signal indicating the search width; the search results circuitry providing an address code for a memory location that is one of the locations that provided the

respective group of match signals of the combined match signal indicated by the priority signals; the memory location storing at least part of an entry of the indicated search width that satisfies the match criterion; the priority encoder circuitry being between the lower part and the upper part of the CAM array on the substrate's surface;

the combining circuitry including:

lower combining circuitry between the priority encoder circuitry and the lower part of the CAM array, responding to match signals from the lower part of the CAM array; and

upper combining circuitry between the priority encoder circuitry and the upper part of the CAM array, responding to match signals from the upper part of the CAM array;

the search results circuitry including:

lower address encoding circuitry between the priority encoder circuitry and the lower combining circuitry, responding to priority signals from the priority encoder signal; upper address encoding circuitry between the priority encoder circuitry and the upper combining circuitry, responding to priority signals from the priority encoder signal; the lower and upper address encoding circuitry together providing one or more most significant bits of the address code;

lower match and suppress selecting circuitry between the priority encoder circuitry and the lower part of the CAM array, responding to match signals and suppress signals from the lower part of the CAM array and priority signals from the priority encoder circuitry, and providing match signals and suppress signals from the

lower part of the CAM array for the combined match signal indicated by the priority signals;

upper match and suppress selecting circuitry between the priority encoder circuitry and the upper part of the CAM array, responding to match signals and suppress signals from the upper part of the CAM array and priority signals from the priority encoder circuitry, and providing match signals and suppress signals from the upper part of the CAM array for the combined match signal indicated by the priority signals; and

least significant bit and array match circuitry that responds to the match signals and suppress signals from the lower and upper match selecting circuitry, to the PE match signal, and to the signal indicating search width, the least significant bit and array match circuitry providing one or more least significant bits of the address code and an array match signal.

36. (Currently amended) A system comprising:

a processor;

an integrated circuit connected for access by the processor, the integrated circuit including a content addressable memory (CAM) that includes:

a CAM array that stores entries in P memory locations that each have a location width; the CAM array providing match signals indicating whether locations have stored entries satisfying a match criterion; and

priority encoder circuitry that responds to the CAM array, providing P/Q priority signals indicating at most one Q group of two or more memory locations, the

group storing an entry that has a search width greater than the location width, the entry having priority and meeting the match criterion.

37. (Currently amended) A system comprising:

a processor;

an integrated circuit connected for access by the processor, the integrated circuit including a content addressable memory (CAM) that includes:

a CAM array that stores entries in P memory locations that each have a location width; the CAM array providing, for each location, a match signal indicating whether the location has a stored entry satisfying a match criterion;

match combining circuitry that responds to the match signals and to a signal indicating one of a set of search widths that are multiples of the location width; the match combining circuitry providing P/Q combined match signals, each indicating a combination of Q match signals for a group of memory locations, the combination depending on the indicated search width; and

priority encoder circuitry that responds to the combined match signals, providing priority signals indicating at most one combined match signal's group of memory locations; the indicated group storing an entry of the indicated search width that has priority and meets the match criterion.

38. (Currently amended) A system comprising:

a processor;

an integrated circuit connected for access by the processor, the integrated circuit including a content addressable memory (CAM) that includes:

a CAM array that stores entries in P memory locations that each have a location width; the CAM array providing match signals indicating whether locations have stored entries satisfying a match criterion;

priority encoder circuitry that responds to the CAM array, providing P/Q priority signals indicating at most one Q group of two or more memory locations, the indicated group storing an entry that has a search width that is a multiple of the location width, the entry having priority and meeting the match criterion; and

selection circuitry that responds to the priority signals, providing selected information for entries stored in the indicated group of two or more memory locations.

39. (Currently amended) A system comprising:

a processor;

an integrated circuit connected for access by the processor, the integrated circuit including a content addressable memory (CAM) that includes:

a CAM array that stores entries in P memory locations; the CAM array providing, for each location, a match signal indicating whether the location has a stored entry satisfying a match criterion;

match combining circuitry that responds to the match signals and to a signal indicating one of a set of search widths; the match combining circuitry providing P/Q combined match signals, each indicating a combination of Q match signals for a

group of two or more memory locations, the combination depending on the indicated search width; and

search results circuitry that responds to the combined match signals and to the signal indicating one of the set of search widths, providing an address code of a memory location in one of the groups of two or more locations, the memory location storing at least part of an entry of the indicated search width that satisfies the match criterion.

40. (Currently amended) A system comprising:

a processor;

an integrated circuit connected for access by the processor, the integrated circuit including a content addressable memory (CAM) that includes:

a CAM array that stores entries in P memory locations that each have a location width and that stores, for each memory location, a suppress value; the CAM array providing, for each location, a match signal indicating whether the location has a stored entry satisfying a match criterion and a suppress signal based on the location's suppress value;

address code circuitry that responds to the match signals and to a signal indicating a search width that is one of a set of two or more multiples of the location width, providing an address code indicating one of a Q group of two or more memory locations, the group storing entries of each of the location widths in the set; the location indicated by the address code storing at least part of an entry of the indicated search width that satisfies the match criterion; and

array match circuitry that responds to the address code and to suppress signals for the group of memory locations; the array match circuitry providing an array match signal that is asserted only when no suppress signal is asserted for the entry.

41. (Currently amended) A router comprising:

input lines that receive data transmissions;

output lines that retransmit data transmissions received on the input lines; content addressable memory (CAM) circuitry that provides information used to retransmit data transmissions on the output lines, the CAM circuitry comprising:

a CAM array that stores entries in P memory locations that each have a location width; the CAM array providing match signals indicating whether locations have stored entries satisfying a match criterion; and

priority encoder circuitry that responds to the CAM array, providing P/Q priority signals indicating at most one Q group of two or more memory locations, the group storing an entry that has a search width greater than the location width, the entry having priority and meeting the match criterion.

42. (Currently amended) A router comprising:

input lines that receive data transmissions;

output lines that retransmit data transmissions received on the input lines;

content addressable memory (CAM) circuitry that provides information used to retransmit data transmissions on the output lines, the CAM circuitry comprising:

a CAM array that stores entries in P memory locations that each have a location width; the CAM array providing, for each location, a match signal indicating whether the location has a stored entry satisfying a match criterion;

match combining circuitry that responds to the match signals and to a signal indicating one of a set of search widths that are multiples of the location width; the match combining circuitry providing P/Q combined match signals, each indicating a combination of Q match signals for a group of memory locations, the combination depending on the indicated search width; and

priority encoder circuitry that responds to the combined match signals, providing priority signals indicating at most one combined match signal's group of memory locations; the indicated group storing an entry of the indicated search width that has priority and meets the match criterion.

43. (Currently amended) A router comprising:

input lines that receive data transmissions;

output lines that retransmit data transmissions received on the input lines;

content addressable memory (CAM) circuitry that provides information used to retransmit data transmissions on the output lines, the CAM circuitry comprising:

a CAM array that stores entries in P memory locations that each have a location width; the CAM array providing match signals indicating whether locations have stored entries satisfying a match criterion;

priority encoder circuitry that responds to the CAM array, providing P/Q priority signals indicating at most one Q group of two or more memory locations, the

indicated group storing an entry that has a search width that is a multiple of the location width, the entry having priority and meeting the match criterion; and

selection circuitry that responds to the priority signals, providing selected information for entries stored in the indicated group of two or more memory locations.

44. (Currently amended) A router comprising:

input lines that receive data transmissions;

output lines that retransmit data transmissions received on the input lines;

content addressable memory (CAM) circuitry that provides information used to retransmit data transmissions on the output lines, the CAM circuitry comprising:

a CAM array that stores entries in P memory locations; the CAM array providing, for each location, a match signal indicating whether the location has a stored entry satisfying a match criterion;

match combining circuitry that responds to the match signals and to a signal indicating one of a set of search widths; the match combining circuitry providing P/Q combined match signals, each indicating a combination of Q match signals for a group of two or more memory locations, the combination depending on the indicated search width; and

search results circuitry that responds to the combined match signals and to the signal indicating one of the set of search widths, providing an address code of a memory location in one of the groups of two or more locations, the memory location storing at least part of an entry of the indicated search width that satisfies the match criterion.

45. (Currently amended) A router comprising:

input lines that receive packets from a communications network;

output lines that transmit packets on the communications network; and

content addressable memory (CAM) circuitry that provides information used to retransmit data transmissions on the output lines, the CAM circuitry comprising:

a CAM array that stores entries in P memory locations that each have a location width and that stores, for each memory location, a suppress value; the CAM array providing, for each location, a match signal indicating whether the location has a stored entry satisfying a match criterion and a suppress signal based on the location's suppress value;

address code circuitry that responds to the match signals and to a signal indicating a search width that is one of a set of two or more multiples of the location width, providing an address code indicating one of a Q group of two or more memory locations, the group storing entries of each of the location widths in the set; the location indicated by the address code storing at least part of an entry of the indicated search width that satisfies the match criterion; and

array match circuitry that responds to the address code and to suppress signals for the group of memory locations; the array match circuitry providing an array match signal that is asserted only when no suppress signal is asserted for the entry.